CMOS WAFER PREPARATION
BEFORE BONDING
Contents

• Rockwood wafer services

• Context
  – Customer’s outsourcing
  – Rockwood thinning flow

• Learning curve
  – Yield loss
  – Breakages
  – Ruling polishing pad lifespan

• Cases study
  – Investigating process issues
  – Microvoids
  – Tape waviness transfer
ROCKWOOD WAFER SERVICES
Rockwood Wafer Services

- Part of Rockwood Specialties Inc - A 4B$ US Listed Company
Rockwood Wafer Services

• Part of Rockwood Specialties Inc - A 4B$
  US Listed Company

• Located near Aix en Provence in France.
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• Diversified business in 2008
  – from only reclaim activities
  – to include Wafer Processing Services
  – which is now making a significant contribution to our business.
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- Diversified business in 2008
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  - which is now making a significant contribution to our business.

- Offering the following typical services
  - Thinning
    - Pre Packaging Grinding
    - SOI thinning.
    - Wafer carriers
    - Bonded wafers
    - Taiko Grinding.
  - Dicing (including DBG process)
  - Wafer re-sizing.
  - Wafer Edge trimming.
  - Polishing and cleaning
    - DSP
    - Bonding Surface preparation
  - And soon Wafer Bonding.
CONTEXT
Context

- **Customer’s outsourcing**
  - Rockwood processes his customer’s CMOS wafers
  - Further used to build sensor
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![Diagram showing processing of individual CMOS wafers](image-url)
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**Context**

**Customer’s outsourcing**

Rockwood's fab (+ subcontractors)
• **Customer’s outsourcing**
  - Rockwood processes his customer’s CMOS wafers
  - Further used to build sensor
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  - Rockwood processes his customer’s CMOS wafers
  - Further used to build sensor
• Rockwood Thinning flow
• **Rockwood Thinning flow**

  - **INSPECTION – Thickness meas.**
    - Final clean room
  - **ADC Si substrate (> 700 µm)**
• **Rockwood Thinning flow**

  **INSPECTION – Thickness meas.**
  Final clean room

  **TAPING**
  Cleanroom 100

  ADC Si substrate (> 700 µm)

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  To protect CMOS side & make the handling safer
• Rockwood Thinning flow

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Final clean room

**TAPPING**
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**GRINDING (→ 200 - 400 µm)**
Cleanroom 10000
2 steps: rough + fine wheel

ADC Si substrate (> 700 µm)

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The wafer is highly warped and the surface damaged
• **Rockwood Thinning flow**

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  CMP / Cleanroom (100)

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  - **FINAL CLEAN & INSPECTION**
    Final clean room (1 – 10)

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**PACKING & SHIPPING**

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**ADC Si substrate**
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- **PACKING & SHIPPING**

---

- ADC Si substrate (> 700 µm)
- To protect CMOS side & make the handling safer
- The wafer is highly warped and the surface damaged
- Next step: bonding on customer’s equipment
Product yield, breakage yield

LEARNING CURVE
Learning

- Yield
Learning

• **Yield**
  - Customer’s data
Learning

• **Yield**
  – Customer’s data
  – « Yield loss » = $\frac{bad\ dies}{total\ dies}$  (per wafer, per batch)
Learning

• **Yield**
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  – « Yield loss » = *bad dies / total dies* (per wafer, per batch)
  – Overlay of C-SAM, electrical measurements, defect measurements
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  - « Yield loss » = \( \frac{\text{bad dies}}{\text{total dies}} \) (per wafer, per batch)
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![Batch average Yield loss (range box)](image-url)
• **Yield**
  – Customer’s data
  – “Yield loss” = bad dies / total dies (per wafer, per batch)
  – Overlay of C-SAM, electrical measurements, defect measurements

---

*Out of 3 production months during ramp up phase*

→ ~ only 25% with yield loss < 10%
Learning

- **Yield**
  - Customer’s data
  - « Yield loss » = *bad dies / total dies* (per wafer, per batch)
  - Overlay of C-SAM, electrical measurements, defect measurements

Out of 3 production months during ramp up phase
→ ~ only 25% with yield loss < 10%

Out of 3 production months 1 year later
→ ~95%
Learning curve

- Ruling pad lifespan
Learning curve

• Ruling pad lifespan

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**FINAL CLEAN & INSPECTION**
Final clean room (1 – 10)
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**FINAL CLEAN & INSPECTION**  
Final clean room (1 – 10)

---

**Step 1: bulk polishing**  
Defect removal, Roughness ~nm

**Step 2: Final polishing**  
Roughness ~A
Learning curve

• Ruling pad lifespan

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\[ T_0: \text{ process set up and frozen with qualification lots (few)} \]
• Ruling pad lifespan

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FINAL CLEAN & INSPECTION
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Ramp up phase: what about lifespan of consumables?
• Ruling pad lifespan

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Final clean room (1 – 10)

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Ramp up phase : what about lifespan of consumables ?

\[ \rightarrow \text{ Technical driver: polishing quality vs time} \]
Learning curve

- Ruling pad lifespan
Learning curve

• **Ruling pad lifespan**
  – Plot of lot yield loss versus consumables information
Learning curve

• **Ruling pad lifespan**
  – Plot of lot yield loss versus consumables information
    • Polishing insert lifespan
Learning curve

- **Ruling pad lifespan**
  - Plot of lot yield loss versus consumables information
    - Polishing insert lifespan
    - Polishing pad preparation conditions
Learning curve

• **Ruling pad lifespan**
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    • Polishing pad lifespan (pad step#1 & pad step #2)
Learning curve

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  - And the winner is…pad lifespan on polishing step #2
### Ruling pad lifespan

- Plot of lot yield loss versus consumables information
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**Learning curve**

**High degradation rate vs std reclaim polishing process**

**Average yield loss**

**Mid lifetime**

**Number of processed hours vs std reclaim lifespan**
Learning curve

- **Ruling pad lifespan**
  - Plot of lot yield loss versus consumables information
    - Polishing insert lifespan
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![Graph showing yield loss versus number of processed hours](image)

- **High degradation rate vs std reclaim polishing process**
- **More likely due to higher wearing rate as caused by sharp edge of thin wafers**
Learning curve

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  - Plot of lot yield loss versus consumables information
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![Graph showing yield loss versus number of processed hours vs mid lifetime](image-url)
Learning curve

• **Ruling pad lifespan**
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    - Polishing insert lifespan
    - Polishing pad preparation conditions
    - Polishing pad lifespan (pad step #1 & pad step #2)
    - Etc..
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Experimental data

CASES STUDY
Case study #1

INVESTIGATING PROCESS ISSUES
Case study #1: investigating process issues

• 1: wafer handling issue on polishing tool
Case study #1: investigating process issues

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    • Sometimes at the end of the polishing cycle the wafer stay “sticked” onto the polishing pad, which is impregnated with slurry
    • Local chemical etching by the basic slurry: the pad groove pattern is “printed” on the wafer
Case study #1: investigating process issues

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→ The problem has been fixed
  Use of vacuum to hold the wafer
Case study #2

MICROVOIDS
Case study #2: microvoids
Case study #2: microvoids

- Microvoids
Case study #2: microvoids

- **Microvoids**
  - Defect located at the bonding interface
Case study #2: microvoids

• **Microvoids**
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  – Small unbonded areas (<0.01 mm²)
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Case study #2: microvoids

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- **Characterization**
Case study #2: microvoids

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• **Characterization**
  – C-SAM & Mic
Case study #3: microvoids

- **Characterization**
  - Profilometry
Case study #3: microvoids

• **Characterization**
  – Profilometry
    • Manufacturing of low adhesion bonded wafers
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    - Wafer mapping (microvoids localization)
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    - Profile on the CMOS wafer
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  – Profilometry
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    → Crater like defect
Case study #3: microvoids

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→ Crater like defect
~ 100 µm wide,
Case study #3: microvoids

• **Characterization**
  – Profilometry
    • Manufacturing of low adhesion bonded wafers
    • Wafer mapping (microvoids localization)
    • Debonding of the pair of wafers
    • Profile on the CMOS wafer
→ Crater like defect
~ 100 µm wide,
~10nm depression /~6nm elevated ring
Case study #2: microvoids
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- Microvoids counts vs process deviations
Case study #2: microvoids

- **Microvoids counts vs process deviations**
  - Microvoids count = number of microvoids / wafer, batch
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- DOE on PRIME wafers (still ongoing)
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  - Influence of the silicon raw material
Case study #2: microvoids

- Microvoids counts vs process deviations
  - Microvoids count = number of microvoids / wafer, batch

- DOE on PRIME wafers (still ongoing)
  - Influence of the silicon raw material
    - Depth variation

Location of the final thin wafer into the original PRIME wafers

<table>
<thead>
<tr>
<th>Original PRIME wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thin wafer</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
Case study #2: microvoids

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- DOE on PRIME wafers (still ongoing)
  - Influence of the silicon raw material
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    - Type of silicon (CZ, FZ)
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- Grinding amount
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  - Increased polishing removals

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- CMOS PROCESS
  - Grinding amount
  - Increased polishing removals
  - Clean (modified cleaning/drying sequence)
  - Type of tape

- CMOS Thinning

- No clear trend: uneven occurrence of microvoids
Case study #3

TAPE WAVINESS TRANSFER
Case study #3: tape waviness transfer

- Final visual inspection on thin wafers
Case study #3: tape waviness transfer

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- **Final visual inspection on thin wafers**
Case study #3: tape waviness transfer

• **Final visual inspection on thin wafers**
  - Wafer warpage: lamp not straight but curved
Case study #3: tape waviness transfer

• **Final visual inspection on thin wafers**
  - Wafer warpage: lamp not straight but curved
  - Reflection is not mirror-like.
    • small “waves” topography on the polished surface
    • mostly random pattern
    • with main direction
Case study #3: tape waviness transfer

• **Final visual inspection on thin wafers**
  
  – Wafer warpage: lamp not straight but curved
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\[ H = \sim 500 - 800 \text{ nm} \]
\[ W = 10 - 15 \text{ mm} \]
\[ W/H = 12000 \rightarrow 30000 \]

Profile

Thin wafer (thinned side)
Case study #3: tape waviness transfer

- Investigation
Case study #3: tape waviness transfer

• **Investigation**
  – Finally focused on 1 step: tape deposition
Case study #3: tape waviness transfer

• **Investigation**
  – Finally focused on 1 step: tape deposition
    • wafer is moved under a roller
Case study #3: tape waviness transfer

• **Investigation**
  – Finally focused on 1 step: tape deposition
    • wafer is moved under a roller
    • Ensuring uniform pressure
Case study #3: tape waviness transfer

• **Investigation**
  – Finally focused on 1 step: tape deposition
    • wafer is moved under a roller
    • Ensuring uniform pressure
  – Demonstration
    • Virgin silicon wafers, 3 taping conditions
    • Std thinning, inspection
Case study #3: tape waviness transfer

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Hologenix – YIS 150
(light deflectivity)
Case study #3: tape waviness transfer

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\[ \text{No tape} \]

Wave pattern is confirmed (shape and orientation) → tape dependent
Case study #3: tape waviness transfer

- Any impact on microvoids?
Case study #3: tape waviness transfer

• **Any impact on microvoids?**
Case study #3: tape waviness transfer

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BONDING with tape

Bonding w/o tape

Top wafer
Bottom wafer
Case study #3: tape waviness transfer

- Any impact on microvoids?

**BONDING with tape**

Top wafer
Bottom wafer

**Bonding w/o tape**

Top wafer
Bottom wafer
TO CONCLUDE
To conclude

- Successful cooperation with CMOS fab
- Enabling
  - Production of sensor with consistent yield though a complex supply chain
  - New technology for our customer
- Building of depth of experience for Rockwood
- Thin wafer (200 µm – 450 µm) processing: tradeoff
  - w/o temporary carrier → fewer thermal and cleaning limitations
  - w/o sacrificial carrier → cheaper
  - But breakage occurrences
THANK YOU